**Computer Logic Design (Section B and E) – Assignment 3**

**Marks: 10**

**Due Date: February 29, 2016. There will be a Quiz on related topics.**

**Hierarchical Implementation of Decoder**

**Note:** Only high level logic diagrams required for questions 2 to 7. Detailed Decoder circuit is not required. **Only use the hardware provided in specification, any single extra gate/decoder not allowed.**

**Question 1:** Construct a 5x32 decoder using four 3x8 decoders and one 2x4 decoder.

**Question 2:** Implement a 6x64 decoder using:

1. only 3x8 line decoders
2. only 2x4 line decoders

**Question 3-5:** Text Book Exercises (Moris Mano 4th Edition): 3-28, 3-29, 3-31

**Implementing Functions using Decoder and External Gates**

**Question 6:** Using one 3 to 8 line decoder, implement the following function

G (A, B, C) = ∑ m (0, 2, 4, 5)

F (A, B, C) = ∑ m (0, 1, 2, 3, 7)

**Question 7:** A combinational circuit is defined by the following functions:

F1= x'.y' + x.y.z'

F2= x' +y

F3= x.y + x'.y'

Implement the circuit with one decoder and external NAND gates only. (Hint: Fill the kmap of each function to find its minterms.)

**Question 8:** Design and implement a 2-level code converter (using one decoder chip and additional NAND logic only) from the BCD to Ringtail (shown below). i.e., the input is a BCD code and the output is Ringtail code. Assume that only the valid BCD input is available.

|  |  |  |
| --- | --- | --- |
| **Decimal** | **BCD Code** | **Ringtail Code**  **BCD-to-Ringtail Code Coverter**  (Combinational Circuit to be designed) |
|  | ***WX Y Z*** | ***ABCDE*** |
| 0 | 0 0 0 0 | 0 0 0 0 0 |
| 1 | 0 0 0 1 | 0 0 0 0 1 |
| 2 | 0 0 1 0 | 0 0 0 1 1 |
| 3 | 0 0 1 1 | 0 0 1 1 1 |
| 4 | 0 1 0 0 | 0 1 1 1 1 |
| 5 | 0 1 0 1 | 1 1 1 1 1 |
| 6 | 0 1 1 0 | 1 1 1 1 0 |
| 7 | 0 1 1 1 | 1 1 1 0 0 |
| 8 | 1 0 0 0 | 1 1 0 0 0 |
| 9 | 1 0 0 1 | 1 0 0 0 0 |

**Decoder with Enable Input**

**Question 9:** RoboNetworks is going to launch a new robot AutoCar. AutoCar receives different signals and performs different functionalities according to the signal received. Following is the detail of signals and functionalities:

|  |  |  |
| --- | --- | --- |
| **(i)** | **Signal** | **Functionality** |
| 0 | 000 | Start Engine |
| 1 | 001 | Switch Front Lights On |
| 2 | 010 | Switch Back Lights On |
| 3 | 011 | Rotate Front wheel right |
| 4 | 100 | Rotate Front wheel left |
| 5 | 101 | Accelerate Front Wheels |
| 6 | 110 | Apply Breaks |
| 7 | 111 | Blow Horn |

Suppose there are eight circuits available in AutoCar namely C0, C1, C2, C3, C4, C5, C6, C7 where Ci performs ith functionality. Further suppose that all these circuits are fully functional.

Signals for AutoCar are received in a decoder, and decoder’s outputs Dis are connected to each circuit Ci. Upon receiving signal 1 from decoder, Ci starts performing its operation. RoboNetworks wants to provide three secret switches in AutoCar

1. Switch L – To control both the front and back lights. The lights will be switched ON only if switch L is ON
2. Switch R – To control rotation of the car. If R is ON only then rotation will work
3. Switch E – To control the engine. If E is OFF Engine will not be started

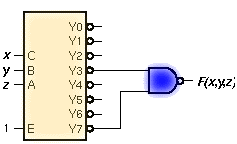
Your task is to design the decoder with these secret switches by following these steps:

1. Make truth table for this decoder
2. Hierarchically implement the decoder

Note: We are not yet considering the circuits to switch off these functionalities of AutoCar.

**Question 10: Short Questions**

1. For a 7-to-128 line decoder, D114 will be ON (1) on input combination \_\_\_\_\_\_\_\_\_\_\_\_\_
2. For a 10-to-1024 decoder, which output will be ON (1) on input 1110011100? \_\_\_\_\_\_\_\_\_\_
3. In an 8-to-256 decoder, value of D96 will be \_\_\_\_\_\_\_\_\_\_\_ on input 1100100.
4. Total \_\_\_\_\_\_\_\_\_\_\_\_\_ AND gates are required for *two-level implementation* of 9-to-512 decoder. (Level-1 for inverters/complements and level-2 for AND gates)
5. How many 1-to-2 line decoders do we need for hierarchical implementation of 9-to-512 decoder? \_\_\_\_\_\_\_\_\_\_\_\_\_
6. A circuit needs to perform different functionalities on 950 input combinations (0 to 950 both inclusive) using decoder. What size of decoder it should use? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
7. What will be the behavior of outputs D951 to D1023 for the decoder used in part (vi)? Explain in two lines.
8. A 3-line to 8-line decoder is connected as shown. Where x, y and z are inputs (z is the least significant input digit) and F is output. Which of the following expressions correctly describes F?



F= Z or F=X or F=Z’ or F=YZ or F=X’